4096-BIT BIPOLAR PROM (512×8) 82S140 (O.C.)/82S141 (T.S.)

DESCRIPTION

The 82S140 and 82S141 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard 82S140 and 82S141 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S140 and 82S141 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S140/141, F or N and for the military temperature range (−55°C to +125°C) specify S82S140/141, F, or R.

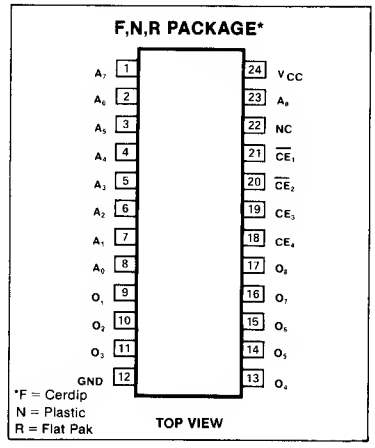
FEATURES

- **Address access time:**
  N82S140/141: 80ns max
  S82S140/141: 90ns max
- **Power dissipation: .17mW/bit typ**
- **Input loading:**
  N82S140/141: −100μA mex
  S82S140/141: −150μA max
- **On-chip address decoding**
- **Output optione:**
  82S140: Open collector
  82S141: Tri-stete
- **No seperete fusing pins**
- **Unprogrammed outputs ere low level**
- **Fully TTL compatible**

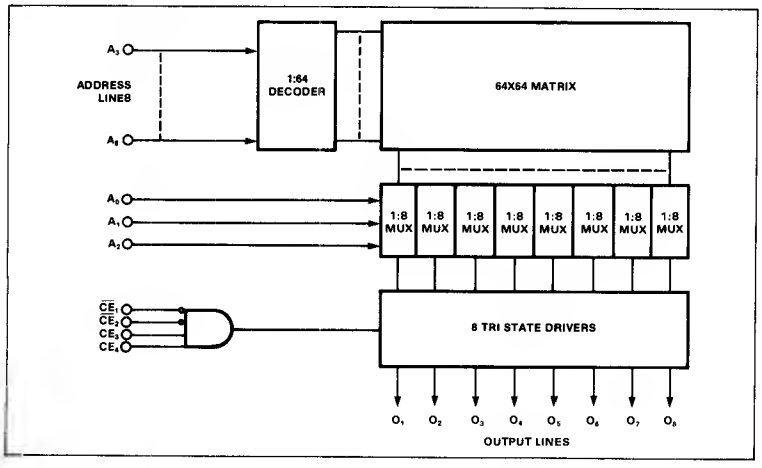
APPLICATIONS

- **Prototyping/volume production**
- **Sequentiel controllers**
- **Microprogremming**
- **Herdwired elgorithms**
- **Control store**
- **Rendom logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S140)	+5.5	
V_O	Off-state (82S141)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S140/141	0 to +75	
	S82S140/141	−55 to +125	
T_{STG}	Storage	−65 to +150	

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DC ELECTRICAL CHARACTERISTICS

N82S140/141: $0°C \le T_A \le 75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S140/141: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1, 2]	N82S140/141			S82S140/141			UNIT
			Min	Typ[5]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2		−0.8	−1.2	
	Output voltage								V
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45			0.5	
V_{OH}	High (82S141)	$\overline{CE}_1$ = Low, $I_{OUT} = -2mA$, $\overline{CE}_2$ = Low, CE_3 = High, CE_4 = High, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			−100			−150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
I_{OLK}	Leakage (82S140)	$\overline{CE}_1$ = High, $V_{OUT} = 5.5V$, $\overline{CE}_2$ = High, CE_3 = Low, CE_4 = Low			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S141)	$\overline{CE}_1$ = High, $V_{OUT} = 0.5V$, $\overline{CE}_2$ = High, CE_3 = Low, CE_4 = Low			−40			−60	μA
		$\overline{CE}_1$ = High, $V_{OUT} = 5.5V$, $\overline{CE}_2$ = High, CE_3 = Low, CE_4 = Low			40			60	
I_{OS}	Short circuit (82S141)[3]	$V_{OUT} = 0V$	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current			140	175		140	185	mA
	Capacitance	$V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

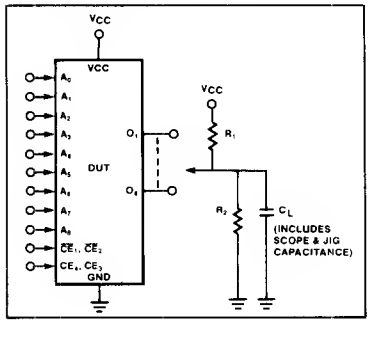
AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S141: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S141: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S141			S82S141			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
Access time									ns
T_{AA}[4]	Output	Address		40	60		40	90	
T_{CE}	Output	Chip enable		20	40		20	50	
Disable time									ns
T_{CD}	Output	Chip disable		20	40		20	50	

NOTES
1. Positive current is defined as into the terminal referenced.
2. All volteges with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical velues are at $V_{CC} = 5V$, $T_A = 25°C$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM